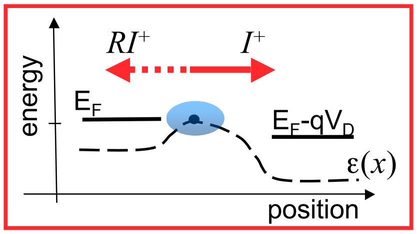
High Mobility Channel Impact On Device Performance

High mobility materials (advantages)

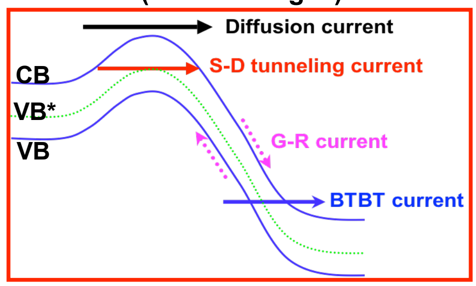


$$I_{sat} = qN_S^{Source} v_{inj} \times \left(\frac{1-R}{1+R} \right)$$

Low $m^*_{transport}$ → High v_{inj}
→ Low R

Increasing μ brings us closer to the ballistic limit

High mobility materials (disadvantages)

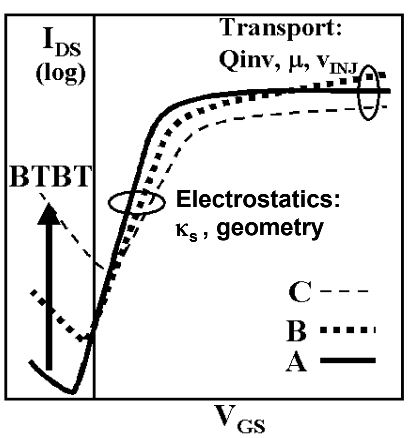


Low E_g → High Leakage Currents
High κ_s → Worse SCE
Low m* → High Tunneling Leakage
→ Low Density Of States

Leakage currents may hinder scalability

High Mobility - Low Leakage

Device performance : I_{off} vs I_{on}



A: Low mobility – low leakage

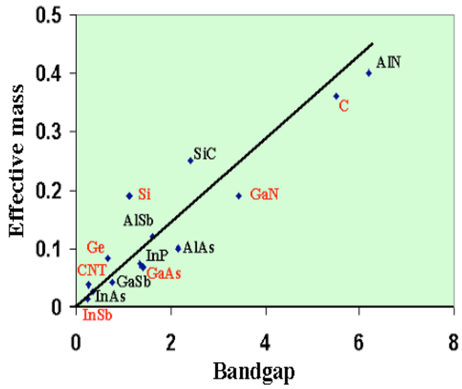
<u>B: High mobility – low leakage</u>

C: High mobility – high leakage

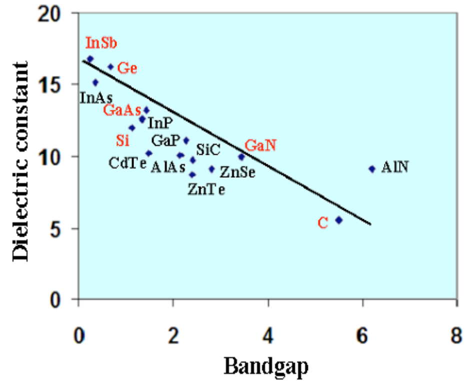
Performance is determined by a *combination* of transport and electrostatics

Picking the Right High-μ Material

Effective mass Vs Bandgap



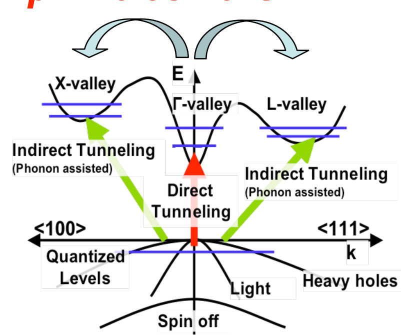
Dielectric constant Vs Bandgap

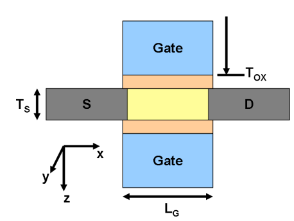


Typical scenario:
- Low Effective Mass
- Small Bandgap
- High Dielectric Constant

Problems with High-μ Materials

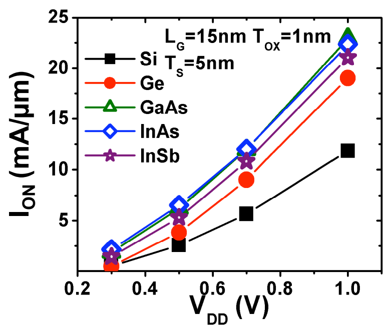
- High mobility materials have:
  - Have low density of states in the Γ-valley, reducing $Q_{inversion}$ and hence drive current.
  - Due to quantization caused by thin body and high surface E-field charge spills into L and X valleys where mobility is low
  - Have small direct band gap which gives rise to high BTBT leakage (except GaAs).
  - Have a high dielectric constant and hence are more prone to short-channel effects.
- We have investigated and benchmarked Double-Gate n-MOSFETs with different channel materials (GaAs, InAs, InSb, Ge, Si) taking into account band structure, quantum effects, BTBT and short-channel effects.

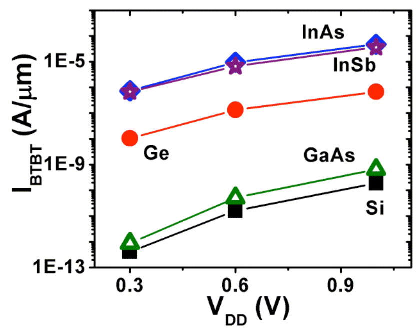




Pethe, Krishnamohan, Kim, Oh, Wong, Nishi and Saraswat, IEDM 2005

Performance vs Scaling



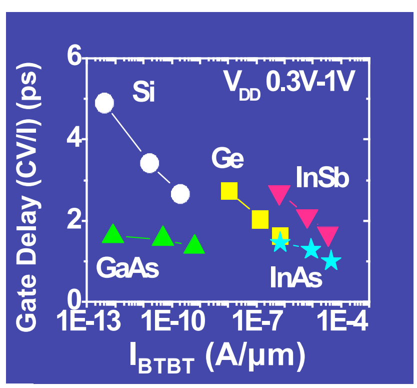


- Ge and III-V materials have higher I_{DS} than Si.
- Band to band tunneling leakage (I_{BTBT}) scales with band gap.

Pethe, Krishnamohan, Kim, Oh, Wong, Nishi and Saraswat, IEDM 2005

Benchmarking Novel Channel Materials for NMOS Performance

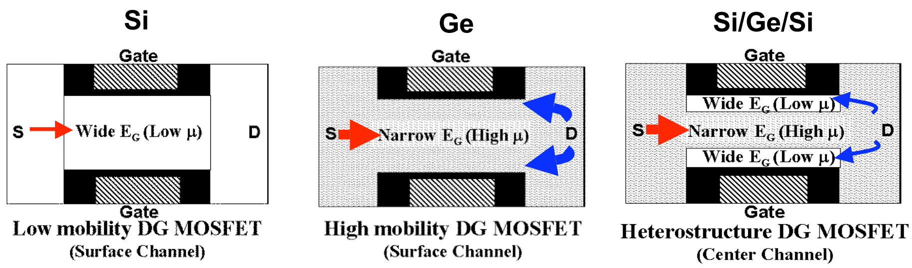
Tradeoffs between <u>performance</u> (CV/I) and <u>static power dissipation</u> (I_{OFF}) for a DG-NMOS with T_{ox} = 1nm and different channel materials



Need innovative structure to combine advantages of a high-µ material for transport and a large bandgap material for leakage

Heterostructure DG MOSFET

Device geometry



Heterostructure: What does it buy us?

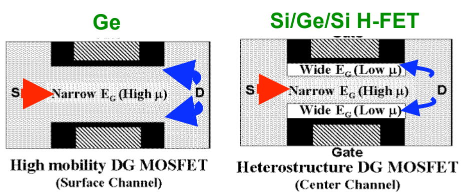
Transport through the high mobility (narrow Eg)

Leak through the wide Eg (low mobility)

T. Krishnamohan et al, IEEE Transactions ED special issue on "Non-classical Si CMOS devices and technologies: Extending the roadmap" (Invited)

Ge/Si Heterostructure PMOS

Materials: Strained Si, Relaxed-Ge or Strained-(Si)Ge?
Device structures: Monomaterial or Heterostructures?



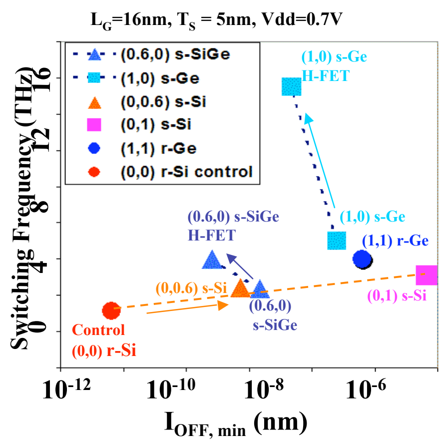
- ✓ Transport through high mobility (narrow Eg)
- ✓ Leak through the wide Eg

Terminology (x,y) for channel material

- x = Ge content in the channel material and
- y = Ge content in an imaginary relaxed (r) substrate to which the channel is strained (s)
- H-FET: heterostructure FET

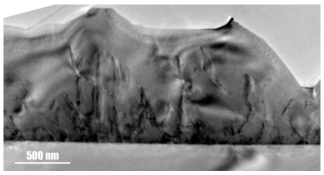
Krishnamohan, Kim, Jungemann, Nishi and Saraswat, VLSI Symp. June 2006

Power-Performance

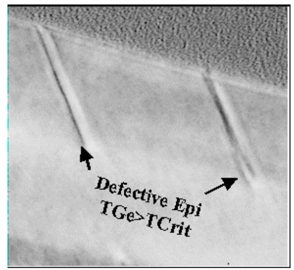


Heteroepitaxial Growth of Ge on Si

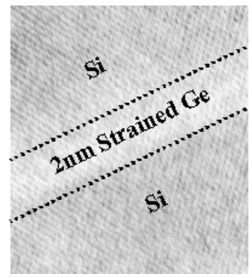
Relaxed-Ge on Si, $T_{Ge} >> T_{crit}$



Strained-Ge on Si $T_{Ge} > T_{crit}$

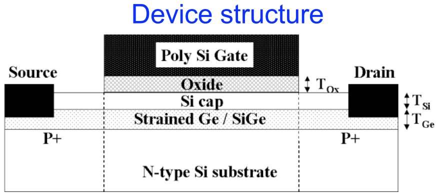


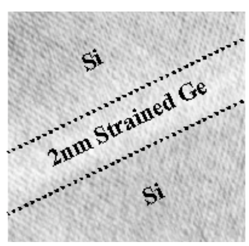
Strained-Ge on Si $T_{Ge} < T_{crit}$



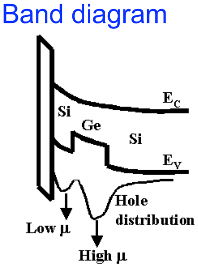
Strained-Ge Bulk PMOS on Relaxed Si

Device structure

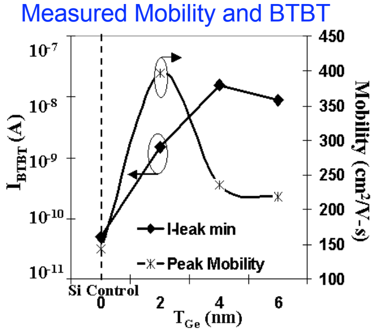




Band diagram



Measured Mobility and BTBT



High mobility due to:

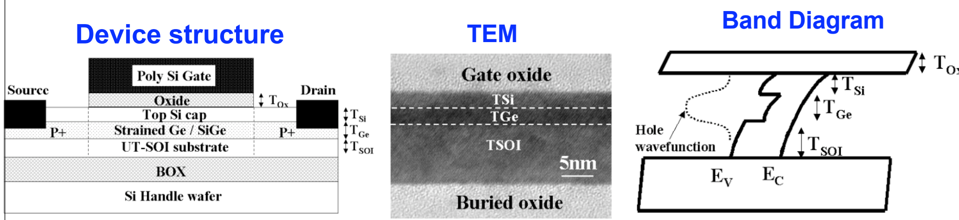
- ✓ Strain in Ge
- ✓ Reduced scattering due to
  - reduced E-field in Ge
  - channel being away from the interface

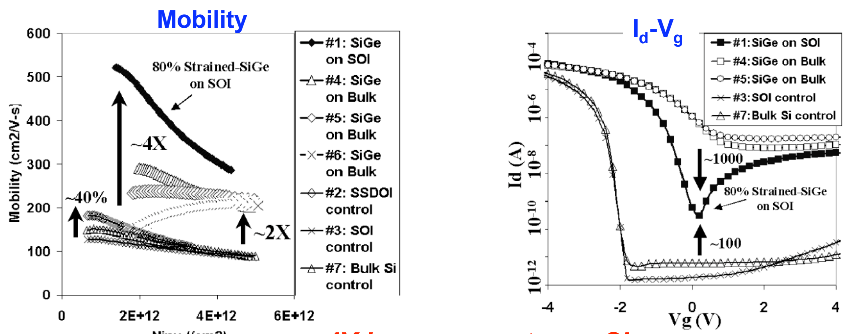
Low S/D leakage due to:

- ✓ Reduced E-field in Ge
- ✓ E_g ⇑ due to confinement of Ge film

Krishnamohan, Krivokapic, Uchida, Nishi and Saraswat, IEEE Trans. Electron Dev., May 2006

Strained-Ge Heterostructure SOI MOSFET

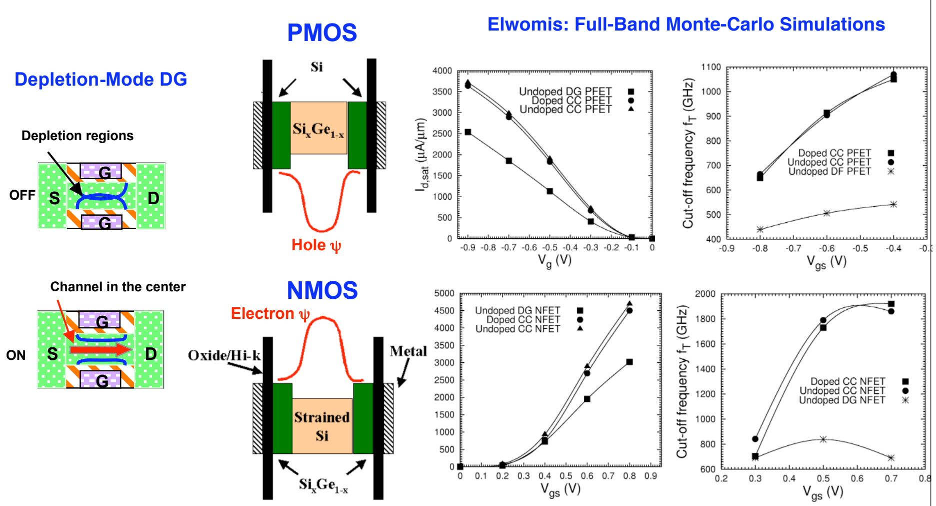




4X improvement over Si

Krishnamohan, Krivokapic, Uchida, Nishi and Saraswat, IEEE Trans. Elec Dev., May 2006

Center Channel Double Gate Heterostructure FET



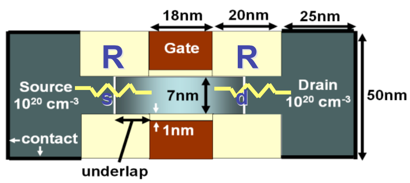
Higher drive current

Higher cut-off frequency

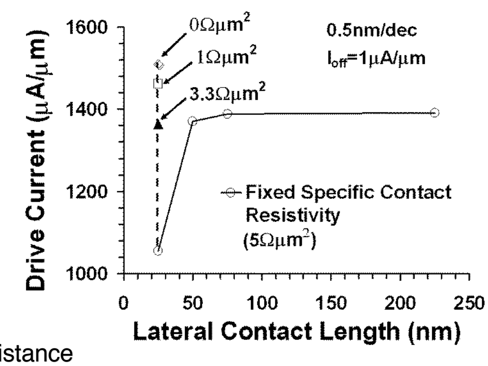
- **Carriers in the center of an un-doped strained-Si or Si_xGe_{1-x} channel**
- **high mobility also due to zero E field, strain, low surface scattering**

Krishnamohan, Kim, Nguyen, Jungemann, Nishi and Saraswat, IEEE Trans. Elec Dev., May 2006

Effect of Extrinsic Resistance on Double Gate FETs



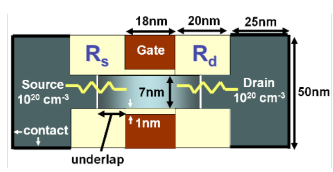
$I_d = K \cdot (V_g - V_{th} - I_d R_s)^{\alpha}$

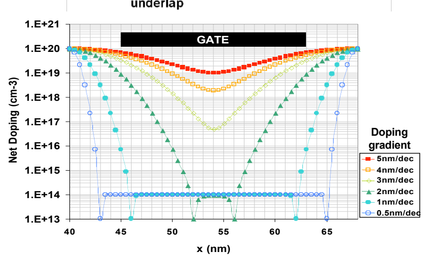


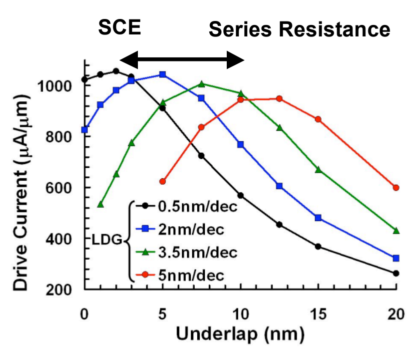
- Ultrathin body ⇒ higher series resistance
- More severe effect in Double-Gate FET
  - Twice I_d flows through same Rs ⇒ higher series drop
- Degradation in I_{ON}
- **Need to reduce parasitic resistance**

Shenoy and Saraswat, IEEE Trans. Nanotechnology, Dec. 2003

Effect of Extrinsic Resistance on Double Gate MOSFETs





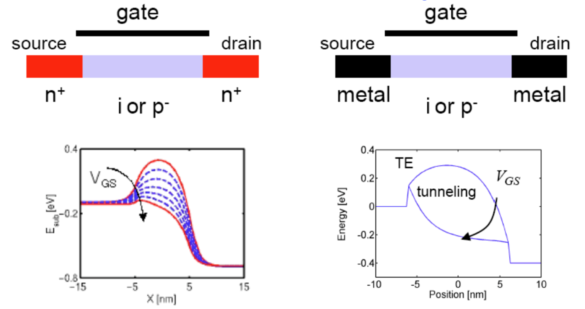


- **Extrinsic resistance reduces gate overdrive ⇒ performance limiter in ballistic FETs**
- **Doping profile too gradual: ⇒ dopants spill into channel ⇒ worse SCE**
- **Doping profile too abrupt: ⇒ large series resistance in extension tip**
- **Extrinsic (S/D) resistance may limit performance in future ultrathin body DGFETs**

Shenoy and Saraswat, IEEE Trans. Nanotechnology, Dec. 2003

Two kinds of transistors

Junction S/D MOSFET | **Schottky S/D MOSFET**



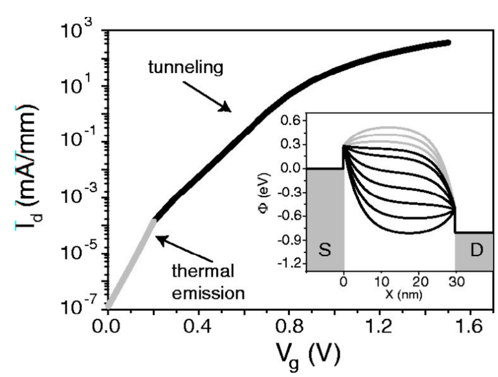
Possible advantages of Schottky S/D MOSFET

- Better utilization of the metal/semiconductor interface
  - Possible option to overcome the higher parasitic resistance
- Modulation of the source barrier by the gate
  - High $V_g \Rightarrow$ barrier thin $\Rightarrow$ tunneling current $\Uparrow \Rightarrow I_{ON} \Uparrow$
  - Low $V_g \Rightarrow$ barrier thick $\Rightarrow$ tunneling current $\Downarrow \Rightarrow I_{OFF} \Downarrow$
- Better immunity from short channel effects

Possible Disadvantage

- I_{ON} reduction due to the Schottky barrier

Schottky Barrier MOSFETs on Ultrathin SOI

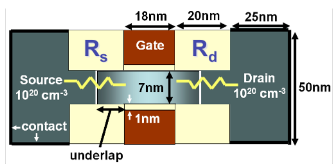


- Simulations of single-gated Schottky barrier MOSFETs on ultrathin silicon on insulator. *T*si=54 nm device at V_{ds}=0.8 V.
- The inset shows the conduction band in the channel for different *Vg* .

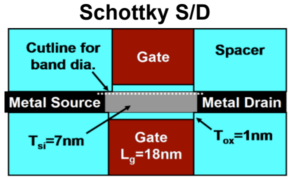
Knoch et al., Appl. Phys. Lett., 14 October 2002

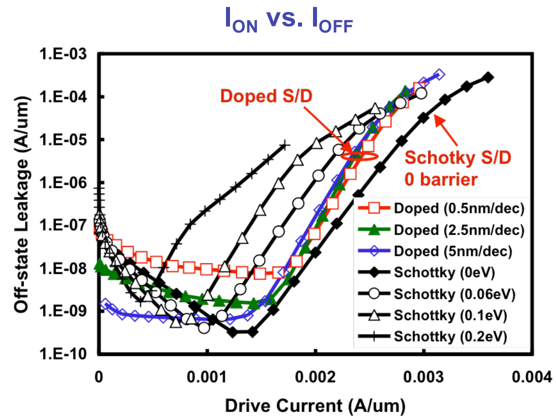
PN Junction vs. Schottky S/D Si DGFET Simulations

PN Junction S/D



Schottky S/D

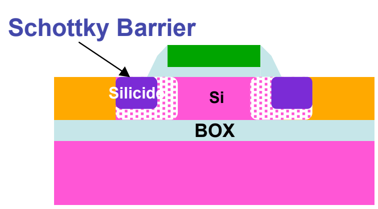




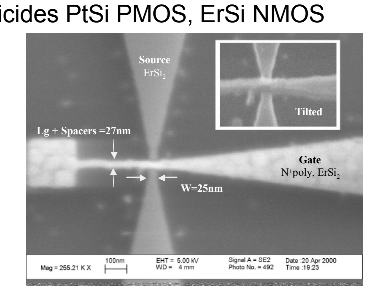
- Low barrier (~0) height metal/semiconductor contacts required to achieve high I_{ON} and low I_{OFF}
- Fermi level pinning makes it difficult to achieve

R. Shenoy, PhD Thesis, 2004

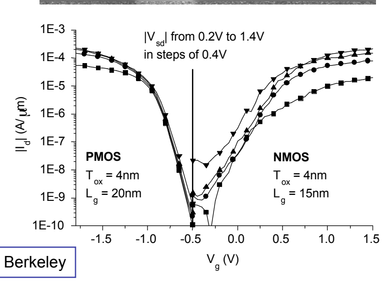
Example of Schottky Barrier MOSFET



L_g~20 nm FETs with Complementary Silicides PtSi PMOS, ErSi NMOS



	PtSi PMOS	ErSi NMOS
Lg	20 nm	15 nm
Tox	4 nm	4 nm
Vg-Vt	1.2 V	1.2 V
Ion	270 uA/um	190 uA/um
Swing	100 mV/dec	150 mV/dec
Ion/Ioff	5E5	1E4
Vt	-0.7 V	-0.1 V

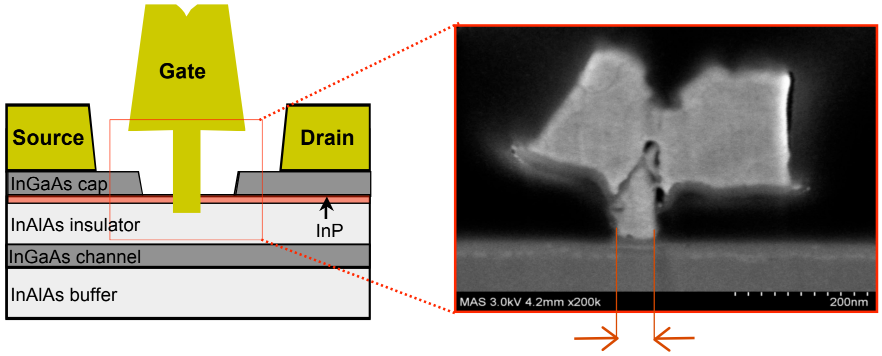


- Metal S/D reduce extrinsic resistance
- Need ultrathin channel, double gate
- Need low barrier technology to ensure high I_{on}

J. Boker et al.- UC Berkeley

60 nm $In_{0.7}Ga_{0.3}As$ HEMTs*

J. A. del Alamo, MIT



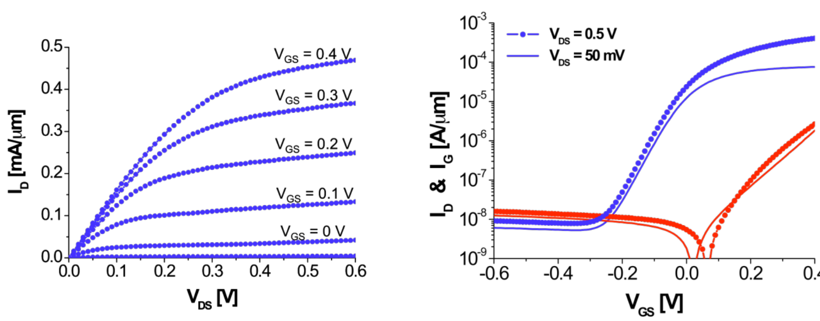
• L_g = ~ 60 nm

Features:

- L_g = ~60 nm gate by e-beam lithography

60 nm InGaAs HEMTs

J. A. del Alamo, MIT

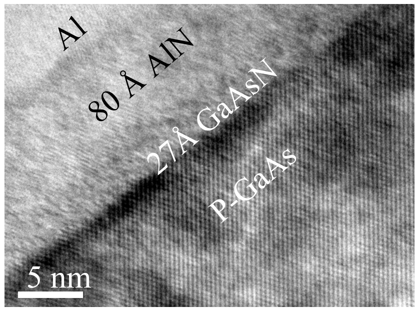


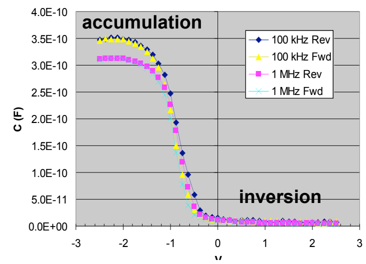
At 0.5 V:

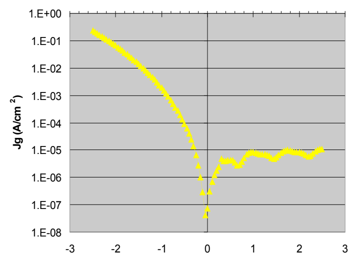
V_T= -0.11 V, S= 70 mV/dec, DIBL= 44 mV/V, I_{on}/I_{off}= 2.7x10^4

MIS Capacitor Stack on GaAs

Fitzgerald (MIT)

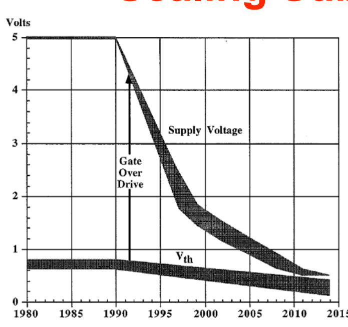




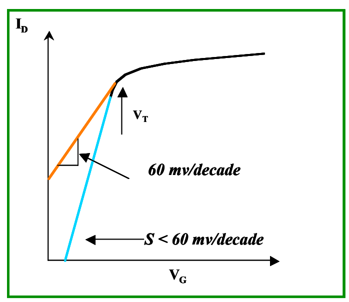


- HFCV shows low hysteresis, little frequency dispersion
- Jg-V curve shows low leakage
- κ of dielectric stack estimated to be ~10.6

Scaling Subthreshold Slope



[NTRS/ITRS data, Plummer *et al*, Proc. IEEE (Mar 2001)]



V_{DD} is scaled for low power,delay → **V_T must scale to maintain I_D**

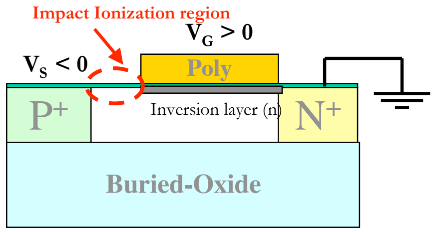
In MOSFET subthreshold slope is limited to kT/q (60mV/dec at 300K)

I_D leakage increases

- **Static power increases**
- **Dynamic-Logic circuits/ latches can lose value**

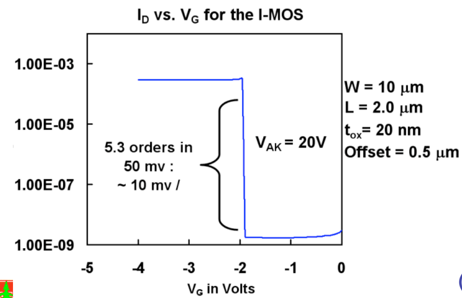
Can we beat the '60mV/dec limit'?

I-MOS

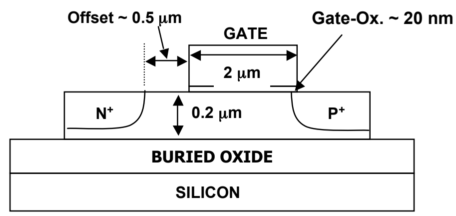


- I-MOS is a gated p-i-n diode and works by channel-length modulation (and hence breakdown modulation).
- 'OFF' state: Low V_G: Longer effective channel length: Lower E-fields: No breakdown.
- 'ON' state: High V_G: Inversion layer: Higher E-fields: Breakdown occurs.

Experimental Results



Device Structure



(K. Gopalkrishnan & J. Plummer, Stanford)

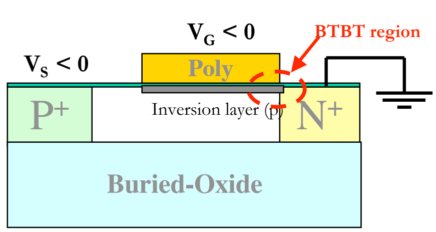
Beating kT/q in MOS Structures

To achieve better than kT/q operation in an insulated gate structure *requires*:

- Carrier injection method with no first order temperature dependence – essentially either impact ionization or tunneling

OR

- Internal gain mechanism
- I-MOS utilizes both approaches: impact ionization and internal gain (avalanche multiplication)

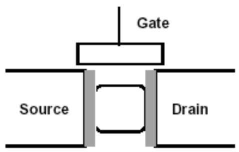


$$J_{tunnel} = \frac{AE^2}{\sqrt{E_G}} \exp\left(-\frac{BE_G^{1.5}}{E}\right)$$

BTBT current: A and B are constants, E is electric field in the tunneling direction, and E_G is bandgap

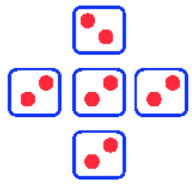
- BTBT has exponential dependence on electric field – *therefore the possibility for steeper than kT/q operation exists*
- Silicon BTBT transistors have consistently shown worse than kT/q subthreshold characteristics
- Practical BTBT transistor will require use of new materials with improved tunneling coefficients.

Seemingly Useful Devices



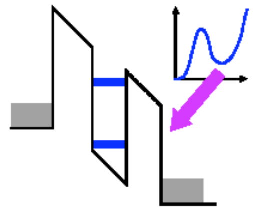
Single Electron Transistors (SET)

Limited Current Drive
Cryogenic operation



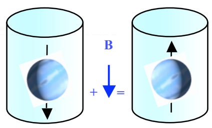
Quantum Dot

Limited Fan-Out
Critical dimension control



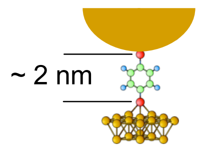
Resonant Tunneling Diode

Challenging fabrication and process integration



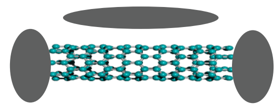
Spintronics

Need high spin injection and long spin coherence time



Molecular Device

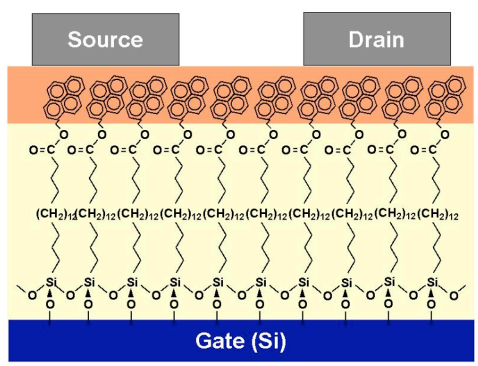
Limited thermal stability
New architectures needed



Carbon Nanotubes

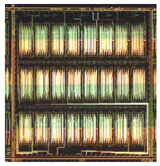
Controlled growth

Organic Insulator / Semiconductor Monolayer



J. Collet et al., APL **76**, 1339 (2000).

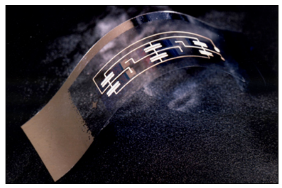
Organic Semiconductors



LSI
(864 Transistors)

B. Crone, A. Dodabalapur et al.
Nature **403**, 521 (2000)

All-Printed Polymer Circuit
Z. Bao / Stanford



Applications

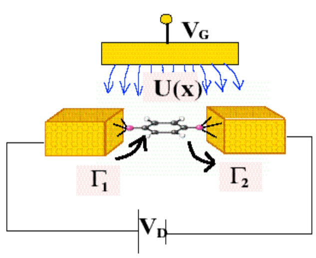
- identification tags
- low-end data storage
- smart cards
- emissive displays
- electronic paper
- distributed computing
- toys, clothes, ...

low-cost, lightweight, rugged, flexible electronics

No competition to Si,
Going where Si can't follow !!

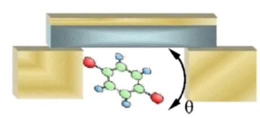
Self-Assembled Monolayer Molecular FET

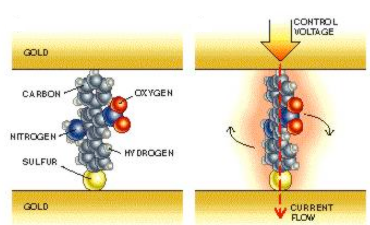
Molecular FETs



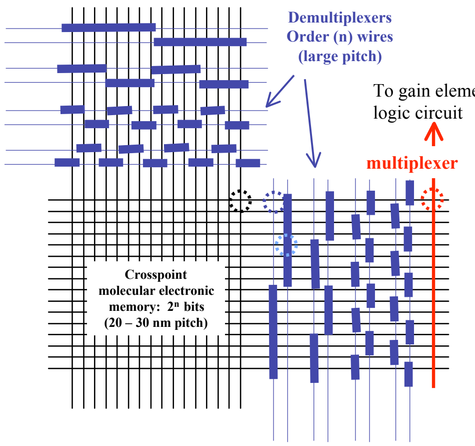
Molecular Length Defines Channel

Molecular Switchs

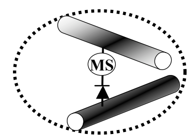


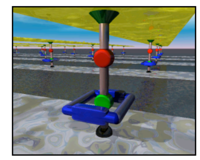


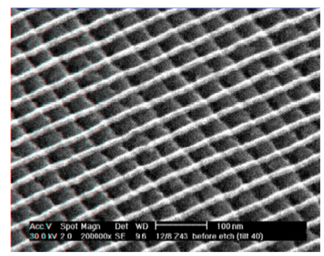
Molecular Electronics Interfaced with Silicon Technology



Molecular Switch





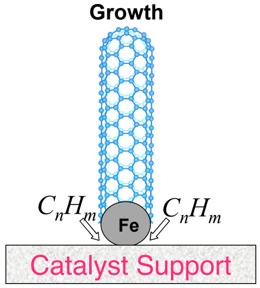


- **Molecular mechanical complexes as solid-state switch elements**
- **Non-traditional patterning techniques to achieve a memory bit (cross-point) density of >10^{11}/cm².**
- **Non-linear, voltage response of molecular switches to latch (amplify) and clock signals by coupling a large molecular circuit with very few CMOS-type amplifiers.**

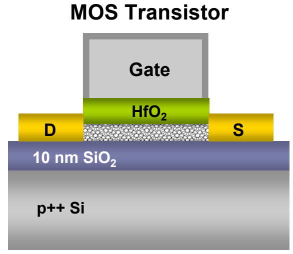
Source: Nicholas Melosh and J. Heath

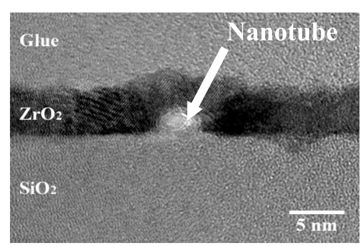
Ballistic Nanotube Transistors

Growth

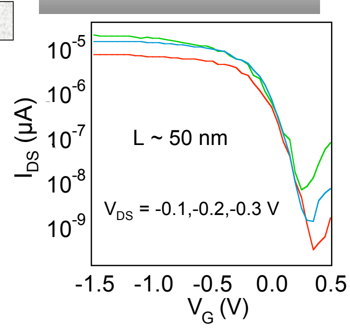


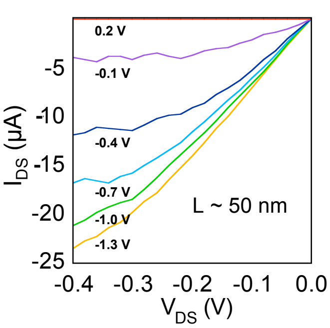
MOS Transistor





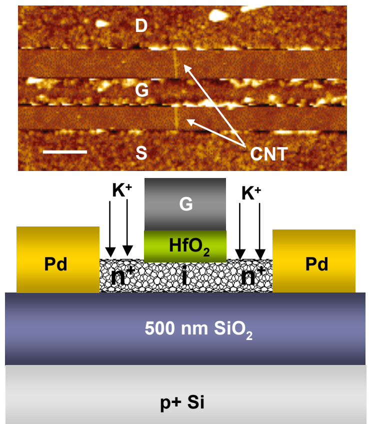
Dai (Stanford)
McIntyre (Stanford)
Gordon (Harvard)
Lundstrom (Purdue)

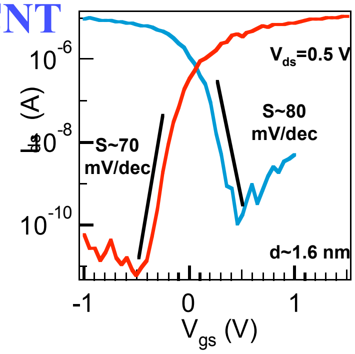


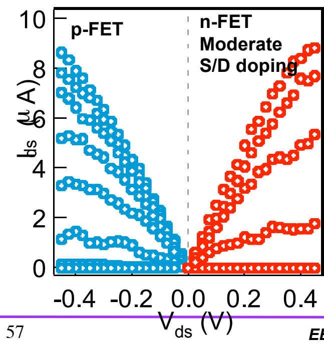


Key Challenge: Low thermal budget controlled growth

High Performance CNT N-MOSFETs

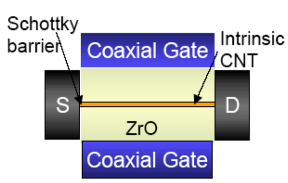






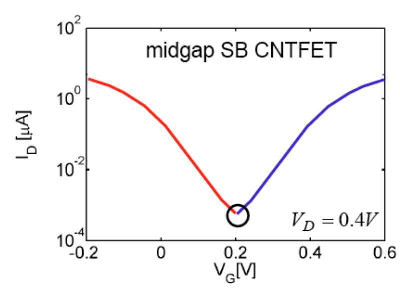
Dai/Gordon/Guo Groups

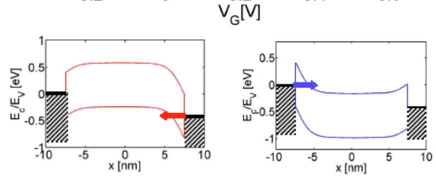
Ambipolar Schottky S/D Nanotube FETs



Schottky barrier CNTFET

Heinze et al, "Carbon nanotubes as Schottky barrier transistors", *PRL*, **89**, 106801,2002



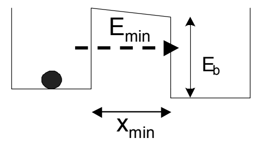


$V_G < V_D/2$
hole conduction

$V_G > V_D/2$
electron conduction

Theoretical Limits to Scaling

- Thermodynamic limit:
  $E_b \geq k_B.T.\ln 2$
- Quantum mechanics
  $\Delta x \,.\, \Delta p \geq h \Rightarrow x_{min}$ (Integration density)
  $\Delta E \,.\, \Delta t \geq h \Rightarrow \tau$ (witching speed)



- Ultimate limit:
  - x_{min} ~ 1.5 nm ➠ 5.10^3 transistors/cm^3
  - Switching speed t_{min} ~ 0.04 ps ➠ 25 Tbits/sec
  - Switching energy E_{bit} = 17 meV
  - Power = 55 nW/bit
- For densely packed, 100% duty cycle devices
  - Total power density = 4.10^6 W/cm^2
- With duty cycle ~1 %, Active transistors ~1 %
  - Total power density = 370 W/cm^2

$$P = \frac{n_{\max} E_{bit}}{t_{\min}}$$

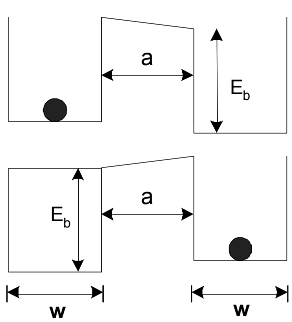
Source: George Bourianoff, Intel

Spin Based Switch

Jim Harris et al. (Stanford)

Charge

ΔE_b(e-) ~1.7×10^{-2} eV

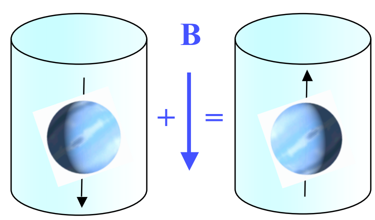


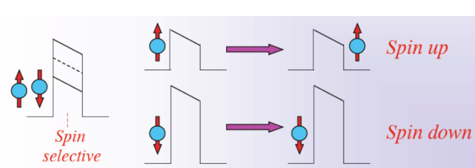
ΔE(spin) << ΔE(e-)

After Mark Bohr, (Intel)

Spin

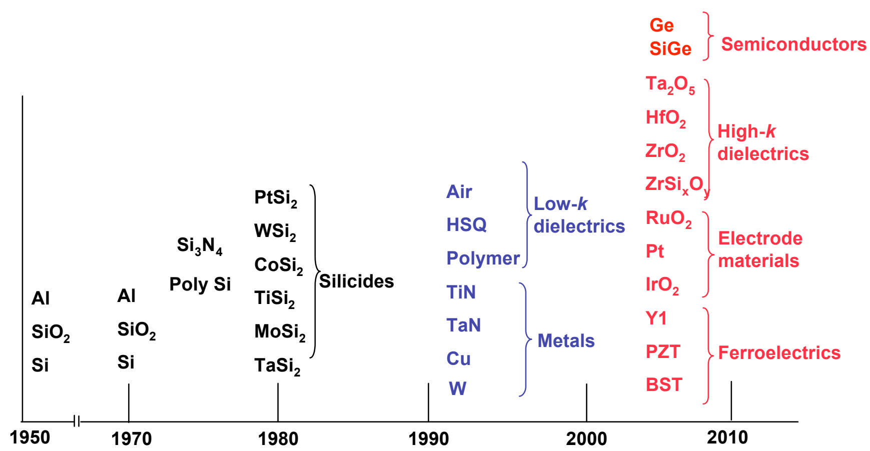
ΔE(spin) ~8.6×10^{-8} eV





Single spin state can be detected by measuring if there is any tunneling current.

New materials



(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

Moore's Law increasingly relies on material innovations

Conclusion: Technology Progression

(After P. Wong)